TECHNICAL EVIDENCE / 05 NOVEMBER 2026

Measured firmware. Not a full FARO claim.

Recovered ELF artifacts and local memory accounting for the native OSH/ FARO test paths executed on three microcontroller families. Traceable measurements, explicit boundaries and no proprietary kernel disclosure.

ARM · 100K
69,516 B
ELF text + data · STM32F446RE

RISC-V · V2 100K
83,708 B
ELF file-backed sections · CH32V307

ESP32-S3 · STEP20
287,668 B
ELF file-backed sections

Scope rule. These are whole-firmware figures (startup, drivers and libraries included), so for the tested native paths they are upper bounds on the linked implementation. They are **not** a measured complete FARO AI installation, and the measurement boundaries differ among target toolchains.

100,000
native validation cycles per family

3 targets
physical ESP32-S3, ARM and RISC-V

05 Nov
local ELF identity and section recovery

What the figures do not mean

A 69 KB ARM firmware is not a 69 KB full FARO architecture. ELF file size, programmed-image span, initialized data, uninitialized BSS, static reservation, peak stack and free heap are distinct measurements. No independent third-party execution or flash readback is claimed here.

01 / TWO NATIVE 100K ARTIFACTS

Authenticated file identities. Readable memory accounting.

STM32F446RE — ARM Cortex-M4

ELF / tool metric	Observed
text (code + read-only classified by GNU size)	**69,200 B**
data (initialized)	**316 B**
bss in `arm-none-eabi-size` (including reserved stack)	**7,376 B**
text + data (file-backed)	**69,516 B**
data + nonstack bss / reserved stack	**6,156 / 1,536 B**

The size utility was executed on **osh_stm32_100k.elf**. Three preserved ELF copies have identical full SHA-256. The corresponding arm 100K BIN is 69,516 B and the programmer historically recorded 67.89 KiB. The exact deployed flash content was not independently read back.

Recovered ARM 100K ELF SHA-256

```
98a420f518d51bbd2d7a797d87df8b2cf825189181d1d7c53ada6ec1d2b95aa1
```

CH32V307VCT6 — RISC-V V2 100K

ELF section classification	Observed
Code + read-only allocated sections	**83,556 B**
Initialized data	**152 B**
Uninitialized BSS (excluding stack)	**5,292 B**
File-backed allocated section sum	**83,708 B**
Static RAM / reserved stack / total incl. reserve	**5,444 / 2,048 / 7,492 B**

The original **OSH_CH32V307_100K_V2.elf** matches the archived full V2/100K SHA-256. RISC-V `size` was not executed; the ELF section table was parsed. Flash memory span and peak stack usage require different measurements. R1's earlier 86,124 B must not replace these V2 figures.

RISC-V V2 100K ELF SHA-256

```
cb9f88f38e755cb82f51fdfe0bf8000ff0963eb774195e1b3b965ae1975c1517
```

02 / ESP32-S3 NATIVE STEP20

Application image, DRAM and measured free memory.

ESP32-S3 — 100K endurance path

Distinct measurement boundary	Value
ELF file-backed allocated section sum	**287,668 B**
Boot log: six application segment sizes	**287,672 B**
Preserved application .bin file size	**287,792 B**
Explicit .dram0.data (initialized)	**13,304 B**
Explicit .dram0.bss (uninitialized)	**13,104 B**
Identified DRAM data + BSS (not all RAM)	**26,408 B**
Internal heap free at 100,000 cycles	**368,691 B**
PSRAM free at 100,000 cycles	**16,774,624 B**
FreeRTOS stack HWM: minimum unused at 100K	**440 B**

Recovered Step20 ELF SHA-256

`41bbe7034913664437e4204819df1facb645767cb752807a207a207928c58540`

The original boot report contains only prefix **41bbe7034...**; it matches this ELF digest's prefix, not a complete archived hash. The app BIN has a separate SHA-256: 4b79d07b06fef50615b3ed54126d49b1b2291be62445125bf5776cca23b7a0d8.

ESP32 accounting correction

Layout-only sections such as `.dram0.dummy`, `.flash_rodata_dummy` and `.ext_ram.dummy` must not be counted as consumed DRAM. The prior overflow-based PSRAM percentage value (0.14%) was incorrect; 64-bit arithmetic on preserved absolute values gives approximately 99.98% free. Physical R2's automatic percentage gate was therefore not a clean full PASS.

03 / REPRODUCIBILITY BOUNDARIES

Strong evidence requires precise limitations.

Identity level

- ARM: exact artifact filename, three byte-identical preserved ELF copies and successful GNU size; deployment readback not recorded.
- RISC-V: preserved V2 100K ELF SHA-256 exactly matches the archived reference; related HEX also matched.
- ESP32-S3: recovered candidate ELF's digest begins with the archived boot-log prefix, but the historic full ELF digest was not logged.

Scope level

- 100K endurance covers specific native state/ decision paths on real silicon, not a complete FARO installation.
- Firmware code size does not measure peak RAM, stack high-water consumption, core power or general intelligence.
- These are owner-side forensic and device records, not independent third-party reproduction.

SOURCE RECORDS

[E1] OSH local binary-discovery JSON, 05 Nov 2026: full SHA-256 calculations, selected ELF sections and ARM GNU size output.
[E2] ARM Physical Validation Report, 03 Oct 2026; ARM Physical Migration Completed: 100K execution, programmed-image observation and hardware identity.
[E3] RISC-V Physical Validation Technical Record, 08 Oct 2026: V2/100K hash, parity and endurance results.
[E4] ESP32-S3 Integrated Native Evidence Report, 18 Sep 2026: Step19 parity, Step20 free-heap, PSRAM, high-water mark and telemetry caveat.
[E5] Original ESP32-S3 Step20 boot log and saved app build: six app segments, partial boot hash and candidate build identity.

Confidentiality boundary

The public report deliberately excludes source code, private Windows paths, build internals, data stores, raw firmware binaries and third-party private identifiers. A binary is not an assurance against reverse engineering once it is accessible. The current FARO Independent Validation SDK offers a public audit path; independently captured physical reproduction remains pending.

FARO = proprietary AI architecture. OSH Global Systems, Inc. = company.