OSH

GLOBAL SYSTEMS, INC.

RESEARCH EVIDENCE / OCTOBER 2026

PHYSICAL RISC-V VALIDATION & CONTROL BENCHMARK

Measured RISC-V silicon execution, physical analog feedback, a matched homeostatic control study and board-level supply observations.



100K
native physical cycles

3 / 3
paired FARO wins

284 us
external scope interval

PUBLIC / NON-CONFIDENTIAL

09 OCT 2026

OSH Global Systems, Inc. | Cross-architecture physical evidence | www.oshsystems.com

01 / EVIDENCE SCOPE

What the evidence establishes

A complete, non-confidential record of native MCU execution, host-driven control and physical instrumentation.

100,000
native MCU cycles

0
ADC / state failures

10.37%
lower mean IAE vs fixed PID

Two distinct experimental boundaries

A / NATIVE EXECUTION

Frozen OSH substrate modules execute **on CH32V307VCT6 silicon**. A native wrapper samples ADC5, advances OSH state/policy and writes DAC1 across 100,000 physical feedback cycles.

B / MATCHED CONTROL EXPERIMENT

FARO V2 and fixed PID run on the **host PC**, controlling the same physical RISC-V DAC-to-ADC plant over UART. These paired tests measure external control behavior; they do **not** establish host-controller execution inside the MCU.

Evidence progression

PC	SUBSTRATE	ESP32-S3	ARM	RISC-V
BASE	PORTABLE	PHYSICAL	PHYSICAL	THIS REPORT

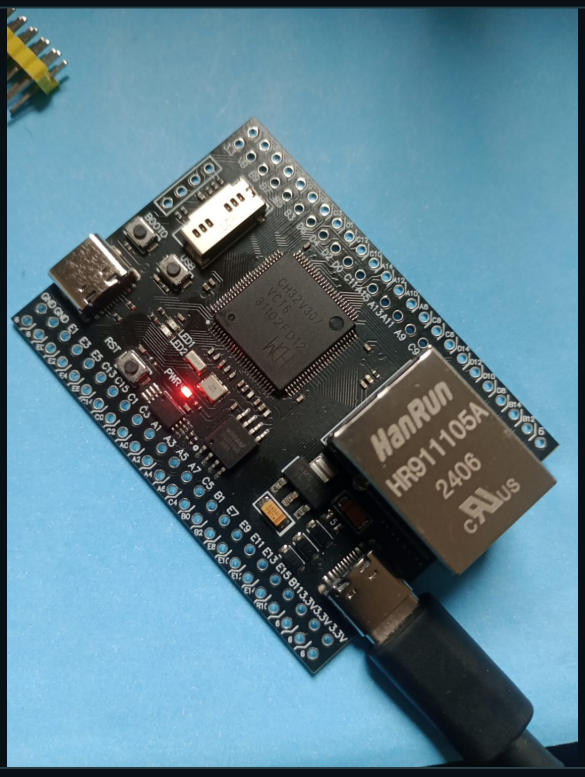
Evidence originates from OSH-run tests; this package is **not an independent third-party replication**. A PASS here is a claim about the declared test gates, not an industrial safety certification.

Additional evidence: direct board supply readings of 4.82 V and 10-11 mA, interpreted on pages 11-12 without attributing board input power to the OSH core.

02 / BENCH ARCHITECTURE

The RISC-V test platform

Physical silicon, directly observed electrical feedback and identity-bearing firmware.



Closed electrical plant - external jumper

TARGET IDENTITY

BOARD
CH32V307VCT6

CORE
QingKe V4F / RISC-V

CLOCK
96,000,000 Hz

CHIP ID
0x30700528

UART
USART1 PA9 TX / PA10 RX

SERIAL LINK
COM4 / 115200 / 8N1

CONTROLLER INPUT
PA5 / ADC_IN5

CONTROLLER OUTPUT
PA4 / DAC1_OUT

DAC1 OUT
PA4

PHYSICAL WIRE →

ADC1 IN5
PA5

The loop is physical: DAC output is wired to an ADC input on the CH32V307 board. No plant simulation or virtual hardware substitutes for the ADC sample.

Native firmware image: SHA-256 `2db7f4dba1893c67...53bb1268`. Firmware programmed and verified via WCHISPTool 4.00; USB-UART used for timestamped host capture.

03 / NATIVE QUALIFICATION

100,000 physical cycles

Acceptance-gated electrical loop and frozen structural parity on actual RISC-V silicon.

Electrical DAC-to-ADC probe

POINT	DAC CODE	ADC READ	ABS. MISMATCH
LOW	512	520	8
MID	2,048	2,048	0
HIGH	3,584	3,571	13

GATE DEFINED BEFORE TEST

ADC must increase monotonically across probe levels, with each absolute DAC/ADC mismatch <= 128 counts. **Measured electrical gate: PASS**.

Native loop qualification

100,000
completed cycles

30 / 30
structural parity

0
ADC / state failures

CHECK	RECORDED RESULT
State failures	0
Invalid actions	0
Timer overflows	0
Actions: INC / HOLD / DEC	36 / 99,934 / 30
Maximum DAC/ADC mismatch	33 counts
Final ref / ADC / abs. error	2662 / 2331 / 331

The 100K PASS establishes the declared physical execution and state-integrity gate. It **does not** mean zero tracking error: the frozen policy has high HOLD occupancy and a measured final residual of 331 ADC counts.

04 / EXPLICIT PERTURBATION

Disturbance & recovery test

Same physical DAC-to-ADC path, a predeclared -240 count disturbance, and MEDIAN5 feedback.

FROZEN TEST DEFINITION

Reference **3071** | pre-disturbance **120** decisions | post-disturbance **120** decisions | DAC perturbation **-240 counts** | maximum action **+/-12** counts | median of five ADC samples.

Recovery is the first of five consecutive post-disturbance observations within the defined error threshold. Minimum required disturbance effect: 150 counts above pre-disturbance baseline.

Measured outcome

METRIC	FARO V2	FIXED PID
Median baseline error	0.5	346.0
Absolute error immediately after disturbance	241	148
Disturbance confirmation	YES	NO
First valid recovery step	22	NOT ESTABLISHED
Post-disturbance IAE	3,239	25,994
Final absolute error	2	123
Predeclared recovery gate	PASS	NOT MET

INTERPRETATION BOUNDARY

FARO V2 passed the declared disturbance-confirmation and recovery gate. **The PID run did not confirm the specified disturbance**: its absolute error fell from a larger existing offset, so the reported step-1 threshold crossing must **not** be called successful recovery.

Post-disturbance IAE values are shown for full disclosure but are not a fair comparison of recovery times when one disturbance-confirmation gate fails.

05 / ENGINEERING CONTEXT

A 70+ year benchmark

Why compare OSH homeostatic control against the long-standing PID family?

THE CLASSICAL REFERENCE / PID

From its mid-20th-century industrial development onward, proportional-integral-derivative (PID) control has remained a widely used foundation of feedback engineering, spanning process automation, motor drives and embedded equipment. Its strengths are practical simplicity, compact implementation, transparent error-based regulation and extensive tuning experience. Poor tuning, saturation, nonlinear plants or changing operating conditions can produce overshoot, slower settling or residual tracking error; **these outcomes are not intrinsic to every PID system.**

THE OSH HOMEOSTATIC PROPOSITION

OSH tests another controller representation: homeostatic structural state and internally derived action instead of a PID coefficient set. In FARO V2, **choose_action receives unsigned need**; the signed target error is deliberately withheld. This is an architectural distinction, **not proof of better tracking** until measured against a declared comparator.

Here FARO V2 runs **on the host**, commanding a physical RISC-V DAC/ADC plant via UART. Independently, frozen OSH modules completed 100,000 cycles **natively on the MCU**. These execution boundaries are not interchangeable.

The testable question

With identical physical plant, sensor-conditioning protocol, reference steps, action limits and alternating test order, **does FARO V2 produce a lower cumulative absolute tracking error than one frozen, documented PID baseline?** Pages 7-8 report the controlled comparison, including unfavorable observations.

Fair-scope statement. The baseline is a conventional PID with fixed predeclared gains, not a proof of globally optimal tuning. Nor do modern learned controllers universally require GPUs: compact neural models can execute on microcontrollers, subject to their own resource and determinism constraints.

CONTEXT SOURCES

[1] Åström & Hägglund, The Future of PID Control, Control Engineering Practice 9 (2001), DOI: 10.1016/S0967-0661(01)00062-4.
[2] David et al., TensorFlow Lite Micro, MLSys 2021, proceedings.mlsys.org (embedded inference context).

06 / COMPARISON PROTOCOL

FARO V2 vs fixed PID

A matched, interleaved experiment on the identical RISC-V physical sensor-actuator loop.

CONTROL TOPOLOGY - EXPLICIT HOST/MCU DIVISION

HOST COMPUTER	UART	PHYSICAL MCU
FARO V2 / PID J4 Python controllers		CH32V307 DAC -> wire -> ADC

The RISC-V MCU supplies real analog input/output. The FARO V2 and PID comparison algorithms run on the host. The independently validated 100K native-OSH run is a different test.

Common protocol

PARAMETER	FROZEN VALUE
Physical plant	Same CH32V307 / PA4 -> PA5
Reference sequence	3,071 / 1,024 / 2,662
Decisions	120 per phase; 360 per run
Physical reset	DAC 2,048; fresh controller state each phase
Sensor acquisition	MEDIAN5 for both controllers
Action limit	+/-12 DAC counts per decision
Pairs	3 interleaved FARO -> PID pairs

FARO V2: no signed target error or PID coefficients enter choose_action. **PID J4**: Kp 0.800 / Ki 0.008 / Kd 0.080; signed error is available.

07 / PHYSICAL RESULTS

Three paired runs, same plant

Cumulative absolute error (IAE) is the declared primary comparison metric: lower is better.

3 / 3
pairs favour FARO

10.37%
mean IAE reduction

0
new UART errors

PAIR	FARO V2 IAE	FIXED PID IAE	FARO LOWER BY
01	107,651	124,072	13.24%
02	114,395	124,081	7.81%
03	111,611	124,109	10.07%
MEAN	111,219	124,087	10.37%

IAE - paired visual comparison



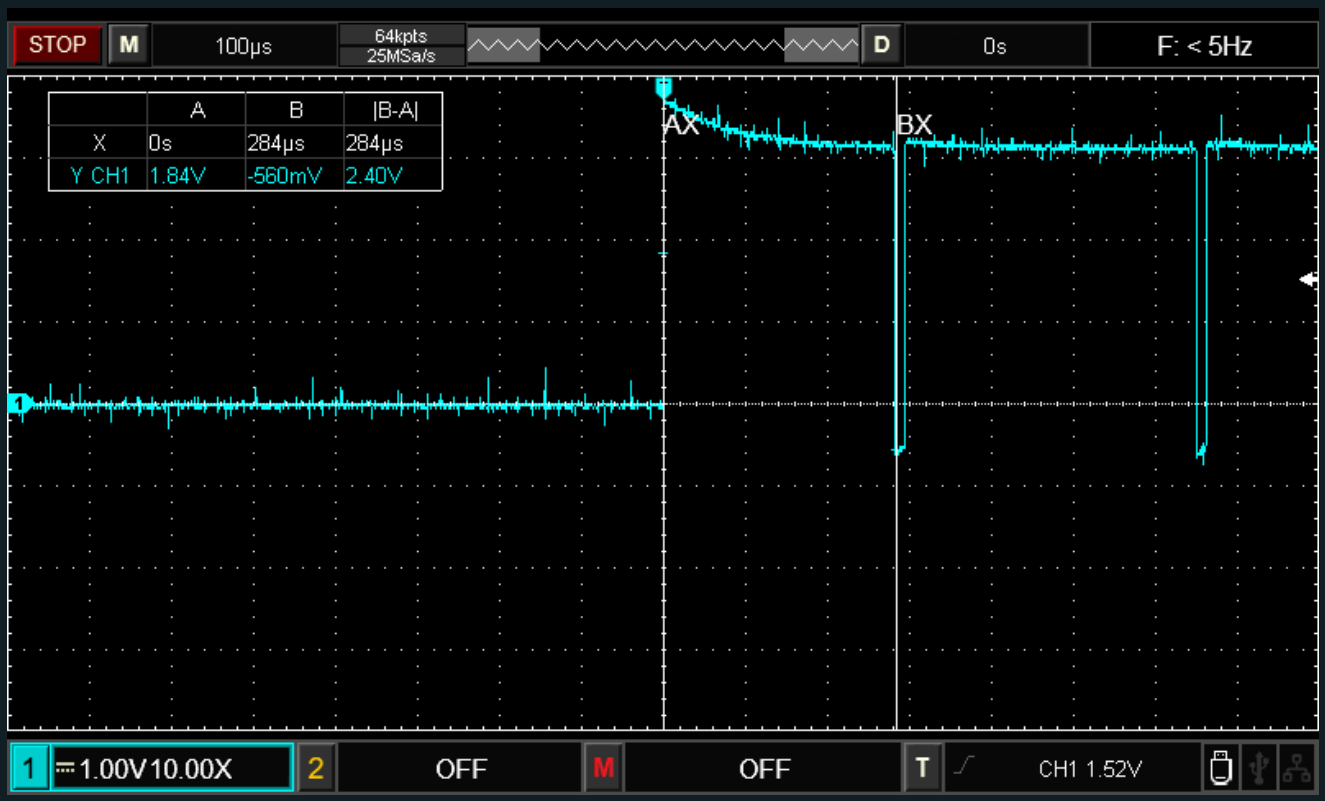
Under this frozen protocol, FARO V2 achieved a mean IAE of **111,219** versus **124,087.33** for the specified fixed PID (10.370384% lower). All six runs completed with 0 ADC failures and no new UART RX errors.

This is a result against one predeclared fixed PID parameter set on one electrical bench plant. It is not a globally optimized-PID claim, and it cannot be generalized to robots, drones or independent industrial plants.

08 / EXTERNALLY OBSERVED TIMING

Original oscilloscope evidence

The original instrument-exported BMP is embedded without retouching or recreated graphics.



INSTRUMENT: UNI-T UTD2052CL+ARG / CH1, DC, 10X / TIMEBASE 100 US/DIV

284 us
cursor A -> B interval

281 us
internal minimum

356.843
internal mean, us

External timing: the exported screenshot displays cursor A at 0 us, cursor B at 284 us and |B-A| at 284 us. This is **one captured marker interval**, not a distribution or MCU-only core runtime. The high interval is bracketed by PA8 under the wrapper-defined ADC-read-to-DAC-write boundary.

TIM2 native firmware recorded route minimum 281 us, maximum 361 us and mean 356.843 us (100,000 samples, 0 overflows). External and internal figures are distinct methods and should not be conflated.

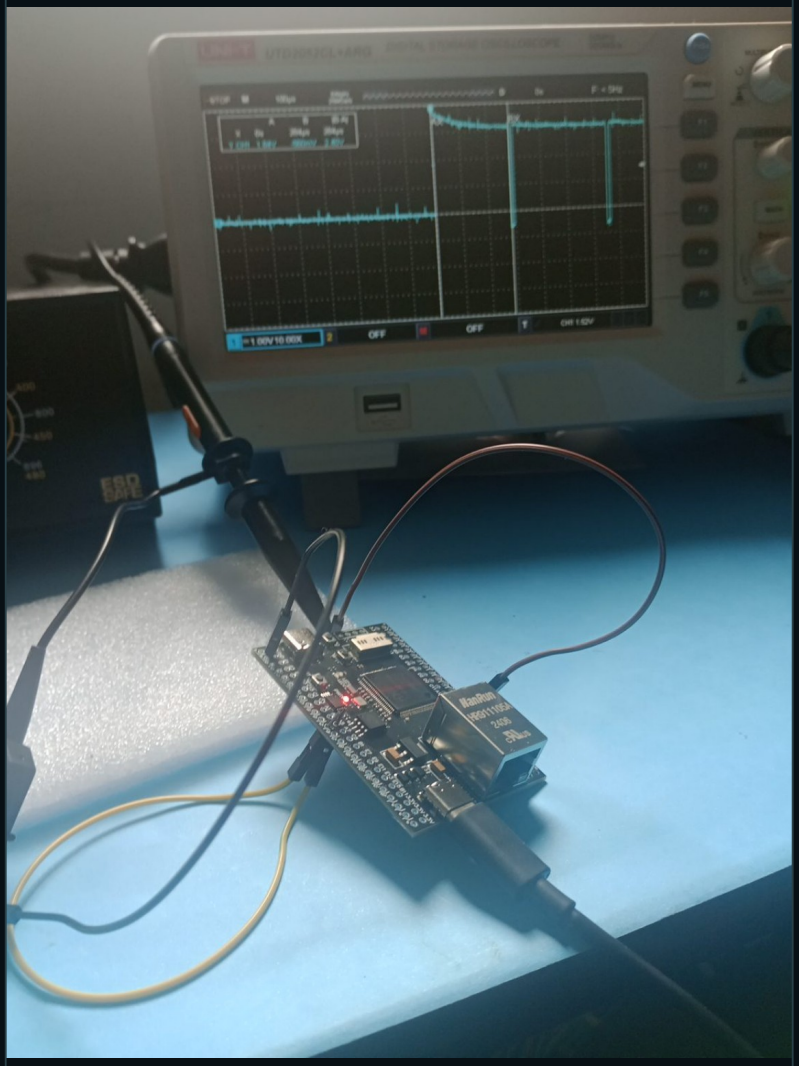
UNMODIFIED RAW BMP / SHA-256

`3bd6bd5dc2eb4423b2bdecb44c78354a07f35dc8c4a87cab7d77793ccde41b6d`

09 / TEST DOCUMENTATION

Instrument and physical setup

A photographic view of the oscilloscope, probe connection and RISC-V board under test.



MEASUREMENT CHAIN

MCU
CH32V307VCT6

MARKER
PA8 / GPIO

INSTRUMENT
UNI-T UTD2052CL+ARG

CHANNEL
CH1

COUPLING
DC / 1 MOhm

PROBE
10X

TIMEBASE
100 us/div

ACQUISITION
Real-Time

CURSOR DELTA
284 us

SUPPLIED BENCH PHOTO - SHA-256

`dd812060b02f2183a820739ba0680fa3fbe20dda6d6cddbdadf5b911557a127b`

The laboratory photograph supports test-setup documentation. The timing claim itself is grounded in the separate, original instrument-exported BMP on the preceding page.

10 / ELECTRICAL POWER

Board-level power observation

Bench supply readout for the complete CH32V307 board under the stated connection.

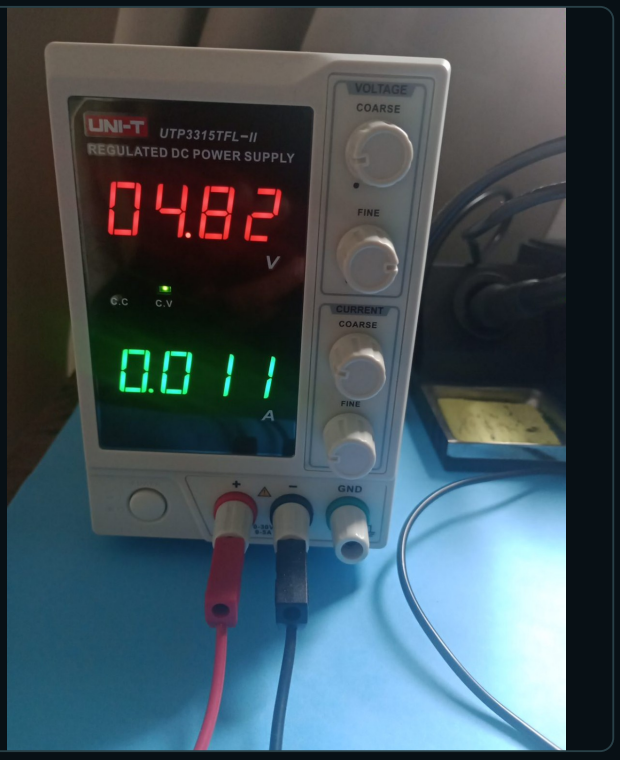
4.82 V
DC supply, CV mode

10-11 mA
displayed input current

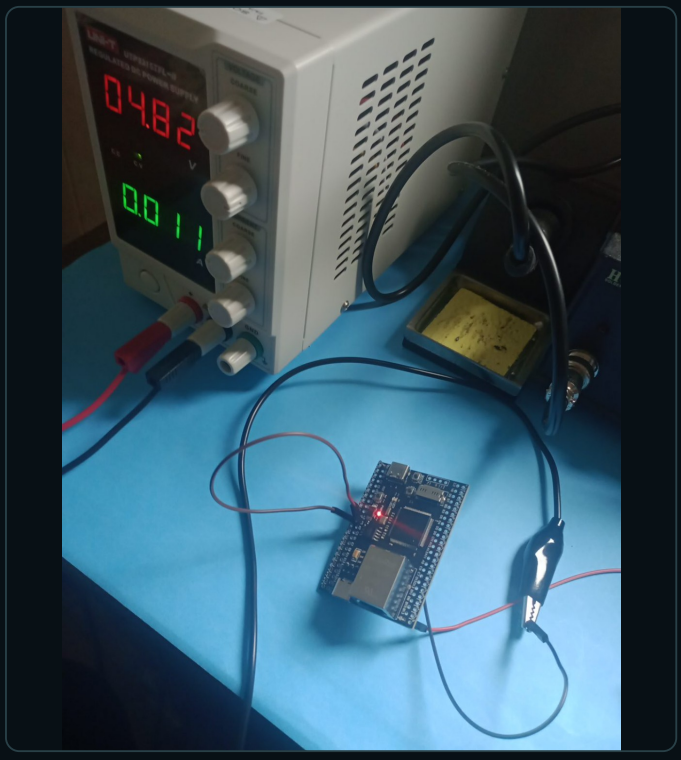
48-53
derived board mW

MEASUREMENT BOUNDARY

With PC USB power disconnected, the **UNI-T UTP3315TFL-II** bench supply indicated **4.82 V** in CV mode and **0.010-0.011 A** across the supplied images and short video. Calculation: **48.2-53.0 mW** of board input, not isolated MCU-core consumption.



LEFT / POWER SUPPLY DISPLAY



RIGHT / LIVE PHYSICAL BENCH

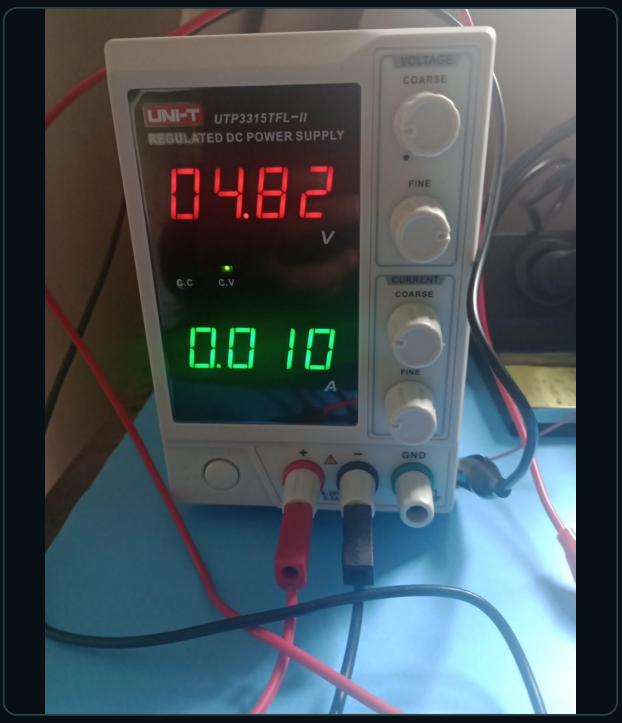
The operator reports a **five-minute** watch with current at 11 mA at the end. The supplied video itself is **9.52 seconds**, so it does not independently substantiate the whole five-minute interval or isolate the 100K active-control period.

11 / POWER RECORD

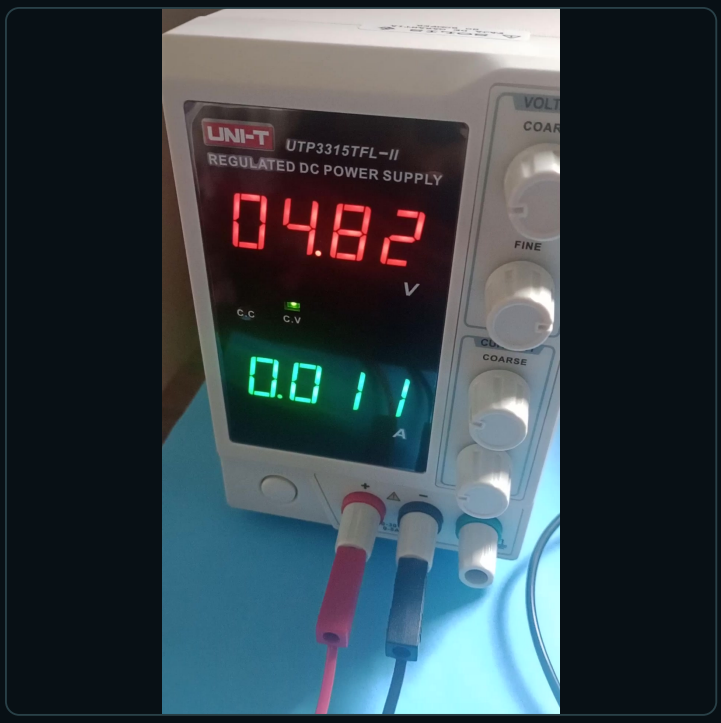
Evidence, resolution & interpretation

A reproducible reporting boundary for low-current bench observations.

Original photo and video evidence



SETUP: 4.82 V / 0.010 A



VIDEO FRAME: 4.82 V / 0.011 A

HOW TO READ THESE VALUES

The supply display changes in **1 mA** increments at this range. Readings are snapshots, not a high-bandwidth current trace. The 100,000-cycle native qualification lasted approximately 37 seconds; an operator-observed 11 mA after five minutes of supply time must **not** be treated as a measured active-cycle average.

POWER EVIDENCE / ORIGINAL BYTES

SOURCE VIDEO / 9.52 S

`ef8c596798ebb5a5955dbefe098fc8c808881deee59e62b77b09bac71a10a397`

SOURCE PHOTO / INITIAL 10 MA

`6fb70c1e533e3983e334bcb33da0f21453230af657ccc5552edff67a38c8c945`

SOURCE PHOTO / 11 MA

`f6f5e9c32f03e77ab76a5a06953490d33d65068fed6aeb449e05318579a58230`

This display is not a continuous power logger. It cannot establish isolated OSH-core power, energy per decision, transients or average current during the active 100K run. Those require a separately instrumented protocol.

12 / PROVENANCE

Cryptographic evidence anchors

SHA-256 identifiers link the public measurements to preserved binary and source artifacts.

OSCILLOSCOPE / ORIGINAL BMP

`3bd6bd5dc2eb4423b2bdecb44c78354a07f35dc8c4a87cab7d77793ccde41b6d`

NATIVE RISC-V FIRMWARE HEX

`2db7f4dba1893c67be1ebcdca9f0b0a6db43484eb9f1fb75e45301bf63bb1268`

RISC-V AUTO-RUN / RAW UART

`c0d003e1561bf876ac1f29b46ad423fc78155eae3444e4b6214be85f6dea51a5`

PHYSICAL DISTURBANCE / RESULT JSON

`8f4ea8a1a1e476f80295d5c64f31a38a893afdbbc9a69ca92933d27a556dcc7f`

MATCHED PHYSICAL COMPARISON / SUMMARY JSON

`ea0ce0d4ef27e76ef46424e73403fe84af961c544aff752b5df2a9fa375cdfe9`

FARO V2 ORGAN (FROZEN)

`18b49da369701cf6d13271a9fa934aca70bce5f8eaae16574781a2537154cf9e`

FARO V2 PRODUCTION STATE (UNCHANGED)

`6b9b5f6fdea3973c0f23d4c196472af4aae052c0325d0bc80d3b4f3587ca3f69`

FIXED PID REFERENCE SCRIPT (ARM-PROVENANCE)

`c43b7cb37ef87d3b4d6c353d3a7be23f439b3b08f2f752b5e305f709d58bc76f`

FARO V2 CONTROLLER REFERENCE SCRIPT

`54e634598c194d03adc183d7654520c59262ae768e477268e8b8a12ff4fbb295`

Hashes are integrity anchors, not substitutes for the underlying data or third-party replication. Original oscilloscope BMP and board-power evidence are separately identifiable (pages 9, 11-12). Native raw UART, controller traces and protocol artifacts can support formal technical diligence.

13 / QUALIFICATION BOUNDARIES

Claims, limits & next gates

For a public evidence portal: explicit separation of observation from extrapolation.

Confirmed within the specified bench

- Native OSH structural parity 30/30 and 100,000 physical CH32V307 cycles, with 0 ADC and state failures.
- Physical DAC-to-ADC probe gate PASS; raw UART trace integrity preserved.
- Host-based FARO V2 disturbance confirmation and recovery PASS (22 decisions), over the physical RISC-V plant.
- Three paired host FARO V2 versus fixed PID experiments on the same RISC-V plant (10.37% lower mean IAE).
- One externally captured execution-marker interval of 284 us, plus board-supply indications of 4.82 V and 10-11 mA (48-53 mW).

Not established by these tests

- That the host FARO V2 comparison controller runs natively on RISC-V; native STEP19 execution was tested separately.
- A valid PID disturbance-recovery comparison under the specified gate: the PID disturbance was not confirmed.
- Global superiority to PID, controller generality across plants, certified safety, or third-party replication.
- Isolated silicon-core power, energy per operation, or an instrument-logged average during the 100K run: not measured.

NEXT INDEPENDENT VALIDATION

Repeat the frozen protocol with independent observers, publish machine-readable traces, log board and MCU power across active and idle phases, and validate a partner-defined plant against predeclared latency, recovery, stability, endurance and energy limits.